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(54) **POWER SEMICONDUCTOR MODULE WITH ASYMMETRICAL LEAD SPACING**

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This patent is subject to a terminal disclaimer.

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(58) **Field of Classification Search**

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See application file for complete search history.

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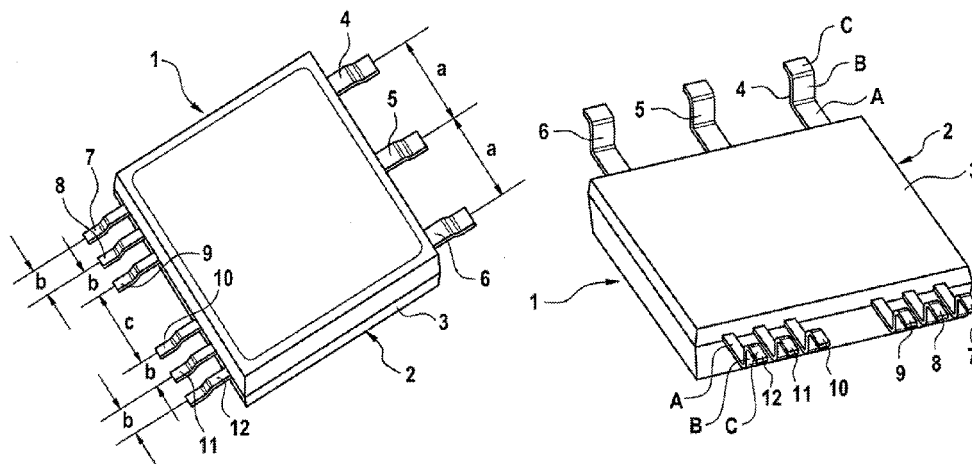
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(57) **ABSTRACT**

A power semiconductor has power terminals arranged in a row at one side of the housing, with control terminals arranged in a row at the other side of the housing. The spacing between adjacent power terminals is greater than the spacing between adjacent control terminals.

**20 Claims, 1 Drawing Sheet**



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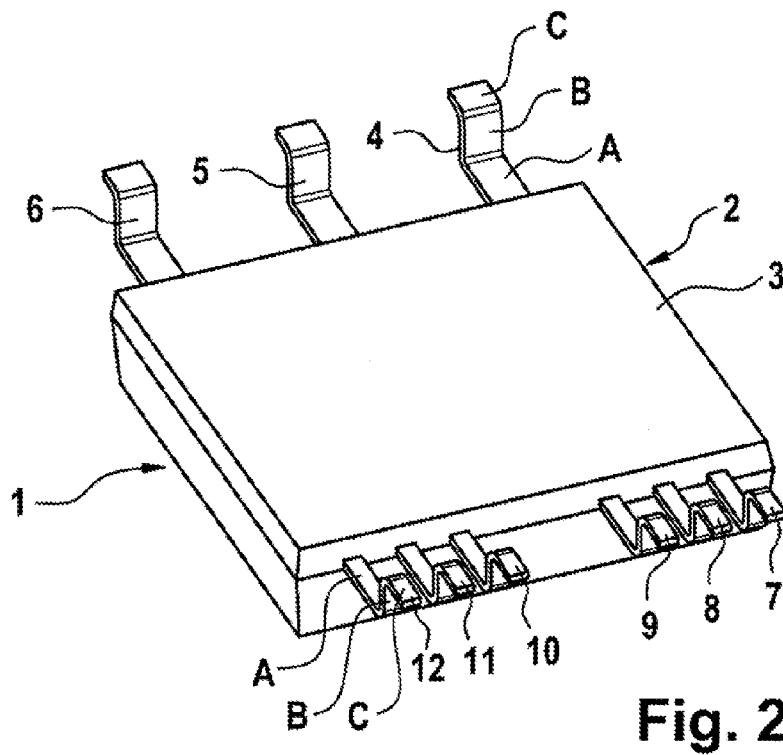
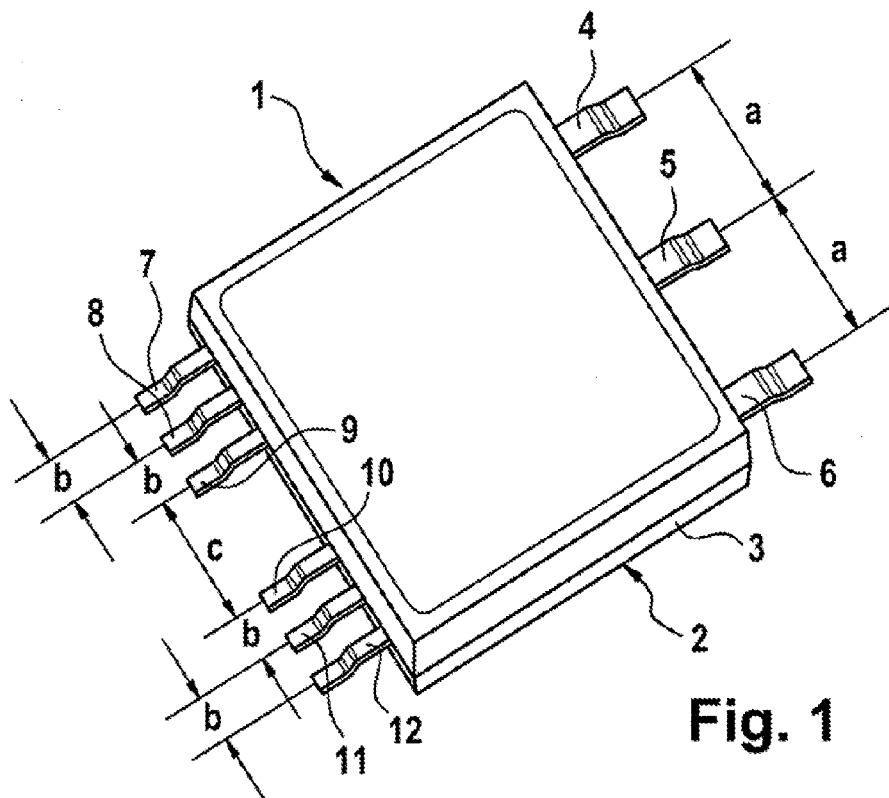
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## POWER SEMICONDUCTOR MODULE WITH ASYMMETRICAL LEAD SPACING

### CROSS REFERENCE TO RELATED APPLICATIONS

This application is a continuation of, and claims priority under 35 U.S.C. §120 from, nonprovisional U.S. patent application Ser. No. 13/472,725 entitled "Power Semiconductor Module With Asymmetrical Lead Spacing," filed on May 16, 2012, now U.S. Pat. No. 9,042,103. U.S. patent application Ser. No. 13/472,725 claims the benefit under 35 U.S.C. §119 from German patent application number 202011100820.0, filed on May 17, 2011, in Germany. The subject matter of each of the foregoing documents is incorporated herein by reference.

### TECHNICAL FIELD

The invention concerns a power semiconductor with a housing, and power and control terminals.

### BACKGROUND OF THE INVENTION

Power semiconductors, which include, for example, well-known IGBTs, are used in various fields of electrical engineering, such as drive control units for electric motors. Power semiconductor modules are known, for example, from EP0513410B1 and DE19646396C2, each of them having an electrically insulating substrate on which a circuit arrangement is placed with power semiconductor components. The substrate forms the base of a plastic housing that encloses the circuit arrangement. The electrical power terminals of the semiconductor components that make contact with the circuit arrangement extend through the housing to the outside. The housing is filled with casting compound to protect the circuit arrangement. Fastening points on the housing are used to screw the module together with a heat dissipating body.

EP1976358B1 describes a power semiconductor that has a carrier board of an insulating ceramic substrate, forming the base of the housing. The carrier board is provided with a metal layer at the top and bottom side, while the top metal layer is structured to form conductor tracks. The conductor tracks are electrically connected to a power semiconductor component, and the power and control terminals of the semiconductor component. The power and control terminals are led out from the housing at the side. The power and control terminals of the power semiconductor are configured as terminals of a surface-mounted component, also known as a SMD (Surface-Mounted Device). The SMD component is mounted on a circuit board.

To maintain the insulation distances required for electrical operation as air and creep distances between the segments of the power and control terminals situated inside the housing and the carrier board, and between the segments of the power and control terminals situated outside the housing and the carrier board, the power and control terminals have a particular configuration. The terminals inside the housing at first extend perpendicularly away from the carrier board, then to the side through the housing to the outside, and finally perpendicular to the circuit board. All power and control terminals have the same spacing.

### SUMMARY OF THE INVENTION

One goal of the invention is to provide a power semiconductor with improved technical properties. The power semi-

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conductor of a preferred embodiment has a carrier board on which at least one power semiconductor component is arranged. The carrier board with the at least one power semiconductor component is at least partly enclosed by a housing. Power and control terminals are electrically connected to the at least one power semiconductor component and led out from the housing.

The power semiconductor of the preferred embodiment has power terminals arranged in a row at one side of the housing, with control terminals arranged in a row at the other side of the housing. The spacing between adjacent power terminals is greater than the spacing between adjacent control terminals. The special arrangement of the power and control terminals at the two sides of the housing provides improved electrical properties, especially when used with high voltages and currents. This also provides insulation distances for air and creep spacing that are larger than in known power semiconductors.

In one preferred embodiment, the power terminals have a larger cross section than the control terminals, thereby making the power semiconductor suitable for switching large currents. In addition to the above arrangement of the power and control terminals, critical air or creep spacings are avoided by the special configuration of the terminals themselves. The power and control terminals in another preferred embodiment have a first segment that extends out from the housing at the side, a second segment that extends from the first segment to the circuit board, and a third segment that extends from the second segment sideways to the outside. Preferably, the individual segments subtend an angle of about 90°.

Several power semiconductor components can be arranged on the carrier board. An especially preferred embodiment has an arrangement of two power semiconductor components on the carrier board. The power semiconductor components have common power terminals, which are arranged on one side of the housing, and separate control terminals, which are arranged on the other side of the housing. The control terminals assigned to the first power semiconductor component are arranged alongside each other in a first row of the housing and the control terminals assigned to the second power semiconductor component are arranged alongside each other in a second row. Preferably, the spacing between the first row and the second row of control terminals is greater than the spacing between adjacent control terminals in the first and second row. With this arrangement, the control terminals are divided into individual groups, each group of terminals being assigned to only one power semiconductor. This assures that the control terminals of different groups, which may differ greatly from each other in electrical potential, are arranged at a sufficient insulation distance, while the control terminals of a group that differ less so from each other in terms of electrical potential are arranged more closely together. The distance between the first row and the second row of control terminals can be the same as, or smaller than, the distance between adjacent power terminals. For mounting on a heat dissipating body, the side of the board facing the heat dissipating body is preferably flush with the housing.

Among the benefits of this structure are that it makes little or no difference as to the type of components of the power semiconductor modules. For example, the power semiconductor modules can be Insulated Gate Bipolar Transistors (IGBTs), but also metal oxide semiconductor field effect transistors (MOSFETs), or other known power semiconductor components.

A sample embodiment of the invention is explained more closely below, making reference to the figures.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates an embodiment of the power semiconductor in a perspective representation from above.

FIG. 2 is a bottom view of the power semiconductor of FIG. 1.

## DETAILED DESCRIPTION

The power semiconductor component according to a preferred embodiment of this invention includes a housing 1, which preferably consists of an insulating material, such as an epoxy compound. The housing 1, however, can also be made at least partly of metal. FIGS. 1 and 2 show the housing of the power semiconductor from different views. Because power semiconductors are well known, we do not herein explain the power semiconductor components or their interconnect structure inside the housing. In the illustrated embodiment, the flat rectangular housing has dimensions of 25 mm×23 mm×5.5 mm.

The housing 1 partly encloses a carrier board 2 of an insulating ceramic substrate, wherein the carrier board 2 forms the base 3 of the housing 1. The carrier board 2 is provided with a metal layer on both the side facing the housing and the side away from the housing. The metal layer facing the housing is structured according to the conductor tracks of a circuit arrangement. On this structured metal layer are arranged, in the present embodiment, two power semiconductor components such as Insulated Gate Bipolar Transistors (IGBTs), not shown in the figures. The power semiconductor components can be soldered, or otherwise attached, to the structured metal layer at the bottom side. On the top side, the power semiconductor components are electrically connected by means of bonding wires to the conductor tracks of the structured metal layer, while the opposite ends of the bonding wires are soldered to the power semiconductor components. The power semiconductor is mounted on a heat dissipating body (not shown), and the base 3 of the housing lies on the heat dissipating body.

Both of the power semiconductor modules have power terminals 4, 5, and 6 and control terminals 7, 8, 9, 10, 11, and 12. The power terminals 4, 5, and 6 of the two power semiconductor components within the package of the illustrated embodiment are assembled to have three common power terminals, which are led out from the housing 1 at the side. Each of the two power semiconductor components, however, has three separate control terminals 7, 8, and 9 in one case and 10, 11, and 12, in the other case, which are likewise led out from the housing 1. The power and control terminals 4 to 12 are bracket-shaped terminals which are preferably configured as terminals of a surface-mounted device (SMD).

All terminals have a first segment A, which extends out from the housing 1 at the side. The first segment A adjoins a second segment B which subtends an angle of about 90° with the first segment. The second segment B passes into an outwardly pointing third segment C, which again subtends an angle of around 90° with the second segment B. The third segment of each terminal is electrically connected to the circuit board (not shown). Typically, the power terminals 4, 5, and 6 differ in their cross section from the control terminals 7, 8, 9, 10, 11, and 12, with the power terminals 4, 5, and 6 having a larger cross section than the control terminals 7, 8, 9, 10, 11, and 12.

The power terminals 4, 5, and 6 are arranged in a row at equal spacings "a" on one lengthwise side of the housing, while the neighboring control terminals 7, 8, 9, 10, 11, and 12 are arranged in a row at the other lengthwise side of the

housing in a spacing "b". The spacing "a" between the adjacent power terminals 4, 5, and 6 is larger than the spacing of the outer power terminals and the edges of the housing. The adjacent control terminals 7, 8, 9, 10, 11, and 12 of the two power semiconductor components form a first group 7, 8, and 9 and a second group 10, 11, and 12, which are arranged alongside each other at the other lengthwise side of the housing 1 in a spacing "c" that is larger than the spacing "b" between the adjacent control terminals of a group. The spacing "c" corresponds to the spacing "a" or can be less than the spacing "a". With both the special arrangement and the special configuration of the power and control terminals, sufficient air and creep distances are created for the electrical operation at high voltage and current, so that the electrical properties of the semiconductor component are improved.

What is claimed is:

1. A power semiconductor module comprising:

a first power semiconductor component having power and control terminals, wherein the first power semiconductor component is disposed on a carrier board;

a second power semiconductor component having power and control terminals, wherein the second power semiconductor component is also disposed on the carrier board, wherein the power terminals of the first power semiconductor component are commonly coupled to the power terminals of the second semiconductor component;

a housing that encloses each of the first and second power semiconductor components, wherein the housing at least partly encloses the carrier board; and

a plurality of electrically conductive leads connected to corresponding ones of the power and control terminals and extending to outside the housing, wherein the electrically conductive leads connected to the power terminals are arranged in a row along one side of the housing, wherein the electrically conductive leads connected to the control terminals are arranged in a row along an opposite side of the housing, and wherein a spacing between adjacent power terminals is greater than or equal to each spacing between adjacent control terminals.

2. The power semiconductor module of claim 1, wherein the electrically conductive leads connected to the power terminals have a larger cross sectional area than the electrically conductive leads connected to the control terminals.

3. The power semiconductor module of claim 1, wherein each of the electrically conductive leads comprises:

a first segment that extends outward from the housing;

a second segment that extends downward from the first segment; and

a third segment that extends outward from the second segment.

4. The power semiconductor module of claim 3, wherein the second segment subtends an angle of approximately 90 degrees from the first segment, and wherein the third segment subtends an angle of approximately 90 degrees from the second segment.

5. The power semiconductor module of claim 1, wherein one of the electrically conductive leads connected to one of the control terminals of the first power semiconductor component is spaced further apart from an adjacent one of the electrically conductive leads connected to one of the control terminals of the second power semiconductor component than the spacing between adjacent electrically conductive leads connected to control terminals of the first power semiconductor component.

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6. The power semiconductor module of claim 1, wherein at least one of the first and second power semiconductor components is an Insulated Gate Bipolar Transistor (IGBT).

7. The power semiconductor module of claim 1, wherein at least one of the first and second power semiconductor components is a metal oxide semiconductor field effect transistor (MOSFET).

8. The power semiconductor module of claim 1, wherein the power terminals of the first power semiconductor component are connected to the power terminals of the second power semiconductor component, and wherein the control terminals of the first power semiconductor component are not connected to the control terminals of the second power semiconductor component.

9. The power semiconductor module of claim 1, wherein the power semiconductor module is a surface-mounted device (SMD).

10. A packaged electronic device comprising:

a housing that has a first side and a second side, wherein the housing encloses a first semiconductor component having power terminals and control terminals and also encloses a second semiconductor component having power terminals and control terminals, and wherein the first side of the housing is opposite the second side of the housing;

a plurality of power terminals arranged along the first side of the housing, wherein each of the plurality of power terminals is a distance A apart from an adjacent one of the plurality of power terminals, wherein the plurality of power terminals extends outside the housing, wherein the plurality of power terminals is connected to the power terminals of the first semiconductor component, and wherein the plurality of power terminals is also connected to the power terminals of the second semiconductor component;

a first plurality of control terminals arranged along the second side of the housing, wherein each of the first plurality of control terminals is a distance B apart from an adjacent one of the first plurality of control terminals, wherein the distance B is less than the distance A, wherein the first plurality of control terminals extends outside the housing, and wherein the first plurality of control terminals is connected to the control terminals of the first semiconductor component; and

a second plurality of control terminals arranged along the second side of the housing, wherein each of the second plurality of control terminals is the distance B apart from an adjacent one of the second plurality of control terminals, wherein one of the second plurality of control terminals is a distance C apart from an adjacent one of the first plurality of control terminals, wherein the second plurality of control terminals extends outside the housing, wherein the second plurality of control terminals is connected to the control terminals of the second semiconductor component, and wherein the distance C is less than or equal to the distance A.

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11. The packaged electronic device of claim 10, wherein each of the plurality of power terminals has a larger cross sectional area than each of the first plurality of control terminals, and wherein each of the plurality of power terminals has a larger cross sectional area than each of the second plurality of control terminals.

12. The packaged electronic device of claim 10, wherein each of the plurality of power terminals, the first plurality of control terminals, and the second plurality of control terminals comprises:

a first segment that extends outward from the housing;  
a second segment that adjoins the first segment; and  
a third segment that adjoins the second segment.

13. The packaged electronic device of claim 12, wherein the second segment subtends an angle of approximately 90 degrees from the first segment, and wherein the third segment subtends an angle of approximately 90 degrees from the second segment.

14. The packaged electronic device of claim 10, wherein the packaged electronic device is a surface-mounted device (SMD).

15. The packaged electronic device of claim 10, wherein the control terminals of the first semiconductor component are not connected to the control terminals of the second semiconductor component.

16. The packaged electronic device of claim 10, wherein the distance A is at least twice as great as the distance B.

17. The packaged electronic device of claim 10, wherein the distance C is less than the distance A.

18. The packaged electronic device of claim 10, wherein at least one of the first and second semiconductor components is selected from the group consisting of: an Insulated Gate Bipolar Transistor (IGBT), and a metal oxide semiconductor field effect transistor (MOSFET).

19. A method comprising:

forming a housing that encloses a first semiconductor component having power and control terminals and a second semiconductor component having power and control terminals such that a plurality of electrically conductive leads extends to outside the housing, wherein a first portion of the electrically conductive leads are connected to the power terminals and are arranged in a first row along one side of the housing, wherein a second portion of the electrically conductive leads are connected to the control terminals and are arranged in a second row along an opposite side of the housing, and wherein a spacing between adjacent electrically conductive leads of the first portion is greater than or equal to each spacing between adjacent electrically conductive leads of the second portion.

20. The method of claim 19, wherein at least one of the first and second semiconductor components is selected from the group consisting of: an Insulated Gate Bipolar Transistor (IGBT), and a metal oxide semiconductor field effect transistor (MOSFET).

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